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ATTORNEY'S DOCKET NO.
062891.0370

PATENT APPLICATION

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APPLICATION FOR U.S. PATENT UNDER 37 C.F.R. § 1.53(b)
TRANSMITTAL FORM



Box Patent Application
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor or Application Identifier:

Riccardo G. Dorbolo

Entitled: METHOD AND SYSTEM FOR REPROGRAMMING
INSTRUCTIONS FOR A SWITCH

Enclosed are:

- ☒ Specification (29 Total Pages)
☒ Drawing(s) (3 Total Sheet(s) of ☒ Formal ☐ Informal)
☒ Combined Declaration and Power of Attorney
☒ Newly executed (original or copy)
☐ Copy from a prior application
(for continuation/divisional only)

- ☒ An Assignment of the invention to Cisco Technology, Inc., is attached.
A separate cover sheet in compliance with 37 C.F.R. § 3.28 and § 3.31 is included
with an Assignment recordal fee of \$40.00 pursuant to 37 C.F.R. § 1.21(h).

☒ Certificate of Mailing

☒ Return Receipt Postcard

Applicant is:

- ☒ Large Entity
☐ Small Entity
☐ Small Entity Statement enclosed
☐ Small Entity Statement filed in prior application.
Status still proper and desired.

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062891.0370

PATENT APPLICATION

2

The accompanying application is:

☒ Original.

☐ Continuation ☐ Divisional ☐ Continuation-In-Part (CIP)

of prior application No. _____ which is hereby incorporated by reference therein.

FEE CALCULATION					FEE
	Number		Number Extra	Rate	Basic Fee
					\$ 690.00
Total Claims:	30	-20 =	10	X \$18 =	\$ 180.00
Independent Claims	6	- 3 =	3	X \$78 =	\$ 234.00
TOTAL FILING FEE =					\$ 1,104.00

X Enclosed is a check in the amount of \$1,104.00 to satisfy filing fee requirements under 37 C.F.R. § 1.16. Please charge any additional fees or credit any overpayment to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P. A duplicate copy of this sheet is enclosed.

Respectfully submitted,
BAKER BOTTS L.L.P.
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Table 1. Demographic characteristics of the study population	
Age (years)	50.0 ± 10.0
Gender (male/female)	100/100
Marital status (married/divorced/separated)	100/100/0
Education (years)	12.0 ± 2.0
Occupation (white/blue)	100/100
Income (USD/month)	1,000 ± 200
Smoking status (smoker/non-smoker)	50/50
Alcohol consumption (yes/no)	20/80
Family history of hypertension (yes/no)	30/70
Duration of hypertension (years)	5.0 ± 3.0
Current antihypertensive treatment (yes/no)	100/0
Medication (ACE inhibitor/CCB/β-blocker/diuretic)	100/0/0/0
Comorbidities (diabetes/cholesterol disease/obesity)	20/30/40
Quality of life score (SF-36)	50.0 ± 10.0
Stress level (low/moderate/high)	30/40/30
Social support (strong/weak)	50/50
Healthcare utilization (regular/irregular)	60/40
Adherence to treatment (high/low)	70/30
Knowledge of hypertension (adequate/inadequate)	60/40
Attitudes towards hypertension (positive/negative)	50/50
Beliefs about hypertension (correct/incorrect)	60/40
Perceived barriers to treatment (yes/no)	30/70
Perceived benefits of treatment (yes/no)	70/30
Healthcare provider's advice (followed/not followed)	60/40
Healthcare provider's support (strong/weak)	50/50
Healthcare provider's education (adequate/inadequate)	60/40
Healthcare provider's attitudes (positive/negative)	50/50
Healthcare provider's beliefs (correct/incorrect)	60/40
Healthcare provider's perceived barriers (yes/no)	30/70
Healthcare provider's perceived benefits (yes/no)	70/30
Healthcare provider's healthcare utilization (regular/irregular)	60/40
Healthcare provider's adherence to treatment (high/low)	70/30
Healthcare provider's knowledge of hypertension (adequate/inadequate)	60/40
Healthcare provider's attitudes towards hypertension (positive/negative)	50/50
Healthcare provider's beliefs about hypertension (correct/incorrect)	60/40
Healthcare provider's perceived barriers to treatment (yes/no)	30/70
Healthcare provider's perceived benefits of treatment (yes/no)	70/30
Healthcare provider's healthcare utilization (regular/irregular)	60/40
Healthcare provider's adherence to treatment (high/low)	70/30
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Healthcare provider's perceived barriers to treatment (yes/no)	30/70
Healthcare provider's perceived benefits of treatment (yes/no)	70/30
Healthcare provider's healthcare utilization (regular/irregular)	60/40
Healthcare provider's adherence to treatment (high/low)	70/30
Healthcare provider's knowledge of hypertension (adequate	

DAL01:542522.1

METHOD AND SYSTEM FOR REPROGRAMMING
INSTRUCTIONS FOR A SWITCH

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of telecommunication switching, and more particularly to a method and system for reprogramming instructions for a switch.

BACKGROUND OF THE INVENTION

The Internet has dramatically increased the potential for data, voice, and video services for customers. Existing circuit-switched telephony systems, however, do not provide the foundation to support the growing need for bandwidth and new services required by both residential and business consumers. As a result, integrated access devices (IADs) have been introduced to support Internet and related technologies as well as standard telephony service for customers.

IADs often combine synchronous and asynchronous transport and switch functionality to multiplex data, voice, and video traffic together onto a single network. Within an IAD, a time division multiplex (TDM) bus is typically used to transport voice and other synchronous traffic between the line cards and a switch core. An asynchronous transfer mode (ATM) bus is used to transport ATM traffic between the line cards and the switch core.

At the switch core, ATM traffic normally arrives asynchronously while TDM traffic arrives in a regular and periodic fashion. Separate ATM and TDM switch hardware are provided to receive and process the ATM and TDM traffic, respectively.

Typically, the TDM traffic is switched by a synchronous switch such as a time slot interchanger (TSI) that cross-connects the TDM channels based on switching instructions in a switching memory. The switching instructions are preprogrammed into the switching memory by a processor and may be altered by the processor in response to protection switching and other events.

For 1:N protection switching, a standby card in the system is provided to be activated in case one of a

number of designated cards malfunctions. When a defect is detected in an operating card and the standby card is activated in its place, the switching memory for the TSI is reprogrammed to write each instruction for the failed
5 card to the instructions for the activated card. This reprogramming of the switching memory involves a large number of microprocessor operations which are relatively time consuming. As a result, protection switching is slowed down in the TSI and may not conform to some
10 telecommunication standards.

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SUMMARY OF THE INVENTION

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The present invention provides a method and system for reprogramming instructions or other routing parameters for a time slot interchanger (TSI) or other switch that substantially eliminates or reduces problems and disadvantages associated with previous systems and methods. In particular, each set of routing parameters in a routing memory is selectively associated with a line card in a redirection memory that can be reprogrammed to switch a routing parameter set for a failed line card to a protect line card with minimal processor operations.

In accordance with one embodiment of the present invention, a method and system for reprogramming instructions for a switch includes programming a redirection memory to associate a routing parameter set in a routing memory for the switch with a first line card. The routing parameter set includes a plurality of routing parameters to be provided to the switch to service the first line card. In response to an event initiating activation of a second line card in place of the first line card, the redirection memory is reprogrammed to associate the routing parameter set in the routing memory with the second line card.

More specifically, in accordance with a particular embodiment of the present invention, the routing parameters are instructions, the routing parameter set is an instruction set and the routing memory is an instruction memory for a synchronous switch. In this and other embodiments, the event may be a failure of the first line card. The redirection memory may be initially programmed to associate a second instruction set in the instruction memory with the second line card. The second

instruction set includes a plurality of instructions to be provided to the synchronous switch to service the second line card. In response to the event initiating activation of the second line card in place of the first line card, the redirection memory is reprogrammed to associate the second instruction set with the first line card. In this way, instruction sets are switched between the line cards. The synchronous switch may be a time slot interchanger (TSI) or other suitable switch.

10 In accordance with one aspect of the present invention, instructions are provided to the synchronous switch by generating a count value including a first portion and a second portion. The second portion is operable to identify a relative location in one of a plurality of instruction sets in an instruction memory for the synchronous switch. The redirection value is determined for the first portion of the count value based on the first portion of the count value. The redirection value identifies an instruction set in the instruction memory. An instruction is read from the relative location in the instruction set based on the redirection value and the second portion of the count value. In a particular embodiment, the count value is a unitary value in which the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant bits (LSB) of the unitary value.

Technical advantages of the present invention include providing an improved method and system for reprogramming routing parameters for a switch, such as instructions for a TSI. In particular, each set of instructions in the instruction memory is selectively

associated with a line card in a programmable redirection memory. The redirection memory may be reprogrammed with minimal processor operations to switch an instruction set of a failed line card to a protect line card. As a
5 result, processor operations and cycles are reduced for protection switching. Thus, protection switching occurs rapidly and within the time required by the telecommunication standards.

Another technical advantage of the present invention
10 includes providing an improved TSI or other suitable switch. In particular, the TSI includes an instruction memory and a redirection memory for associating instruction sets with the line cards serviced by the TSI. The redirection memory adds a level of indirection to the
15 TSI that allows N:1 protection switching reprogramming to be performed with only two processor operations. Accordingly, the TSI operates more efficiently and within telecommunication standards.

Other technical advantages of the present invention
20 will be readily apparent to one skilled in the art from the following figures, description, and claims.

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BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals
5 represent like parts, in which:

FIGURE 1 is a block diagram illustrating a telecommunications system in accordance with one embodiment of the present invention;

10 FIGURE 2 is a block diagram illustrating a detailed view of a node in the telecommunications system of FIGURE 1 in accordance with one embodiment of the present invention;

FIGURE 3 is a block diagram illustrating details of the synchronous switch of FIGURE 2 in accordance with one
15 embodiment of the present invention;

FIGURE 4 is a block diagram illustrating a details of the instruction system of FIGURE 3 in accordance with one embodiment of the present invention;

20 FIGURE 5 is a block diagram illustrating details of the redirection memory of FIGURE 4 in accordance with one embodiment of the present invention; and

FIGURE 6 is a flow diagram illustrating a method for reprogramming instructions for the time slot interchanger
25 (TSI) of FIGURE 3 in accordance with one embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 illustrates a telecommunications system 10 in accordance with one embodiment of the present invention. The telecommunications system 10 transmits voice, data, video, other suitable types of information, and/or a combination of different types of information between source and destination points.

Referring to FIGURE 1, the telecommunications system 10 includes customer premise equipment (CPE) 12 and integrated access devices (IADs) 14 connecting the CPE 12 to a network 16. The IADs 14 communicate voice, data, and/or video traffic between the CPE 12 and the network 16.

The CPE 12 includes standard telephones, modems, computers, dataphones, and other devices capable of generating traffic for transmission in the telecommunications system 10. The CPE 12 is connected to the IADs 14 through a communication link 20. The communication link 20 may be a T1 line, conventional twisted pair cable, fiber optic, or other suitable type of wireline and/or wireless link.

The network 16 may include portions of the Internet, one or more intranets, other wide or local area networks, telephony switches such as a class 5 switch and the like. In a particular embodiment, the network 16 includes backbone routers 18 at its borders for communicating with the IADs 14. In this embodiment, the backbone routers 18 may be Cisco 12000 routers. It will be understood that different types of backbone routers 18 as well as different types of devices capable of directing,

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switching, or otherwise routing traffic may be used in connection with the present invention.

FIGURE 2 illustrates details of the IAD 14 in accordance with one embodiment of the present invention. In this embodiment, the IAD 14 is implemented in a card shelf configuration with functionality of the device distributed between discrete cards connected over a backplane. The backplane includes one or more transmission busses connecting line cards and switch cards. It will be understood that other types of access devices and/or nodes may be used in connection with the present invention.

Referring to FIGURE 2, the IAD 14 includes line cards 40, a switch core 44, and a backplane 46. The line cards 40 and switch cards of the switch core 44 each include hardware and software stored in random access memory (RAM), read only memory (ROM), and/or other suitable computer-readable memory for performing switch and other functionality of the cards. The line cards 40 are each a discrete card configured to plug into the backplane 46. Used herein, each means every one of at least a subset of the identified items. The switch core 44 comprises one or more discrete switch cards also configured to plug into the backplane 46.

The line cards 40 include customer line cards 48 and network line cards 50 that communicate traffic with network 16. Each line card 48 and 50 includes one or more external interfaces, or ports, one or more internal interfaces, and a traffic processor. The ports receive ingress traffic from an external line and/or transmit egress traffic received by the internal interfaces from the switch core 44. The internal interfaces transmit

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ingress traffic received by the ports from the external links and receive egress traffic from the switch core 44. The internal interfaces communicate with the switch core 44 over the backplane 46. The traffic processor is preferably local to the line card 40 and includes hardware and software for processing telephony voice (DS-0) synchronous transmission signal (STS-N) traffic, integrated services digital network (ISDN) traffic, synchronous optical network (SONET) traffic, synchronous digital hierarchy (SDH), asynchronous transfer mode (ATM), and/or other suitable traffic.

The switch core 44 includes a synchronous switch 52 that performs time division multiplex (TDM) switching and an ATM switch 54 that performs cell-based switching. The synchronous switch 52 provides cross-connection for telephony connections, SONET SPEs, other synchronized traffic, and asynchronous traffic segmented into time slots. The ATM switch 54 switches ATM cell traffic, ATM adaption layer (AAL) cell traffic, and segmented packet traffic. The switch core 44 may also convert traffic between the TDM and ATM realms to establish cross-connection between line cards 40.

The switch core 44 or other suitable element of the IAD 14 may implement protection switching for the device 14. In a particular embodiment, 1:N protection switching is provided in the device. In this embodiment, one or more protect line cards 40 provide protection for a number of active line cards 40. When a defect is detected in an active line card 40, the line card 40 is deactivated and the protect line card 40 activated in its place. As described in more detail below, switching

instructions are modified within the switch core 44 to correspond to the change in status of the line cards 40.

FIGURE 3 illustrates the synchronous switch 52 in accordance with one embodiment of the present invention. In this embodiment, the synchronous switch 52 switches 16 bit traffic based on 36 bit instructions. The 16 bit time slots allows channel associated signaling (CAS) and other overhead and/or superframe information to be transported and switched with the traffic. The 36 bit instructions allow sub-channel traffic to be consolidated, expanded, and switched within the synchronous switch 52. Further details regarding the 16 bit time slots and 36 bit instructions are provided in co-owned U.S. Patent Application Serial No. 09/452,828, entitled Time Slot Interchanger (TSI) and Method for a Telecommunications Node filed December 1, 1999, which is hereby incorporated by reference.

Referring to FIGURE 3, the synchronous switch 52 includes a time slot interchanger (TSI) 80 and an instruction system 82 that provides instruction words to the TSI 80. Based on the instruction words, the TSI 80 performs cross connections between TDM channels of the line cards 40.

The TSI 80 is coupled to the line cards 40 through a time slot bus (TSB), an input TSB timing, synchronization, and protection (TTSP) interface 90 and an output TTSP interface 92. The input TTSP interface 90 includes a serial-to-parallel converter for each line card link and a concentrator 94 that multiplexes together the parallel stream produced by the serial-to-parallel converters. In the illustrated embodiment, the concentrator 94 generates a 16 bit composite stream that

is input into the TSI 80. The TSI 80, in turn, generates a 16 bit output stream that is passed to the output TTSP interface 92. The output TTSP interface 92 includes an expander 96 that de-multiplexes and serializes the TSI 80 output for each line card link. The de-multiplex output is serialized by the serializers for transmission to line cards 40.

The TSI 80 is coupled to an exchange memory 100 through a bank selector 102. The exchange memory 100 includes exchange RAM 0 and exchange RAM 1 between which the TSI 80 alternates each frame cycle. In particular, egress traffic is stored into one of the exchange RAMs each frame while traffic from a previous frame is read out of the other exchange RAM during the frame. The bank selector 102 alternately selects each of the exchange RAMs for receiving ingress traffic written to the exchange memory 100 by the TSI 80 or providing egress traffic read from the exchange memory 100 by the TSI 80.

The instruction system 82 is coupled to the TSI 80 and provides program switching instructions to the TSI 80 in the form of instruction words. The instruction words provides read and write operations for transferring DS-0 and other traffic between time slots of the line cards 40. In this way, the TSI 80 cross-connects TDM channels in the IAD 14.

FIGURE 4 illustrates the instruction system 82 in accordance with one embodiment of the present invention. In this embodiment, the instruction system 82 includes an instruction memory 110, instruction counter 112, redirection memory 114 and a controller 116. It will be understood that the instruction system 82 may include

additional or disparate suitable elements without departing from the scope of the present invention.

Referring to FIGURE 4, the instruction memory 110 is a RAM or other suitable memory or set of memories capable of storing and providing instructions to the TSI 80. The instruction RAM 110 includes an instruction set 120 for each line card 40 of the IAD 14. Each instruction set 120 includes an instruction 122 for each time slot of the associated line card 40. Thus, the instruction set 120 provides cross-connection information for each time slot of the line card 40. In an exemplary embodiment in which the IAD 14 includes 32 line cards that each have 256 time slots per frame, the instruction RAM 110 includes 32 instruction sets 120 that each have 256 instructions for a total of 8,192 instructions. It will be understood that the size and number of the instruction sets 120 may be suitably varied to correspond to the configuration of the IAD 14.

The counter 112 generates an incrementing count value that, as redirected by the redirection memory 114, sets the order of instructions 122 to be read from the instruction RAM 110 by the TSI 80. The count value is incremented linearly during each frame cycle of the TSI 80 from an initial value that absent redirection represents the first instruction 122 in the first instruction set 120 to a final value that absent redirection represents the last instruction 122 of the last instruction set 120. The total count value corresponds to the number of instructions 122 in the instruction RAM 110. In this way, each instruction 122 is read from the instruction RAM 110 to the TSI 80 during each cycle of the TSI 80. In the exemplary embodiment,

the count value is a binary value incremented from zero to 8,191 to read the 8,192 instructions 122 of the instruction RAM 110.

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The count value includes a first portion operable to
5 identify the instruction set 120 and a second portion
operable to identify the particular instruction 122 in
the instruction set 120 to be read. In the exemplary
embodiment, the count value is a 12 bit binary value
including most significant bits (MSB) 0-4 that identify
10 the instruction set 120 and least significant bits (LSB)
5-11 that identify the location of an instruction 122
relative to an instruction set 120. The MSBs are passed
to the redirection memory 114 for redirection in
accordance with the current state of the IAD 14 while the
15 LSBs are passed to the instruction RAM 110 to identify an
instruction 122 in an instruction set 120 identified by
the redirection memory 114 based on the MSBs received
from the counter 112. It will be understood that the
counter 112 may otherwise suitably identify an
20 instruction set 120 and an instruction 122 and that the
count value may be otherwise suitably partitioned for
redirection of the instruction set 120 without departing
from the scope of the present invention. For example,
the counter 112 may include two or more component
25 counters that generate discrete values that together
represent the incrementing count value. The counter 112
may be any type of device capable of generating a signal
that selects each of the instructions 122 in the
instruction RAM 110 in a programmable order.
30 The redirection memory 114 is a register bank or
other suitable type of memory, software, and/or hardware
capable of associating an input instruction set 120

identified by the counter 112 with an output instruction set 120 to be read from in the instruction RAM 110, and thus associates each line card 40 with an instruction set 120. The redirection memory 114 adds a level of
5 indirection to the TSI 80. As described in more detail below, the redirection memory 114 allows instruction sets 120 to be selectively associated with the line cards 40 to facility protection switching in the IAD 14 within the time required by telecommunication standards. The
10 redirection register 114 may also allow an instruction set 120 to be associated with a plurality of line cards 40 by listing it as the output instruction sets 120 for the line cards 40. Similarly, instruction sets 120 may be skipped by omitting them in the redirection memory
15 114.

The controller 116 programs the redirection memory 114 to establish and alter associations between the line cards 40 and the instruction sets 120. The controller 116 may be any suitable type of processor running on
20 program instructions or other logic capable of programming the redirection memory 114 in response to protection switching events within the IAD 14. In one embodiment, the controller 116 may be a processor in the switch core 44 that dynamically programs the redirection
25 memory 114.

FIGURE 5 is a block diagram illustrating the redirection memory 114 in accordance with one embodiment of the present invention. In this embodiment, the redirection memory 114 is implemented as a register bank
30 130. The redirection register bank 130 includes an input set of registers 132 and an associated output set of registers 134. The input registers 132 include an

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	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2
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prior to or during operation of the IAD 14. At step 154, failure of the working line card 40 is detected. Next, at step 156, the protect line card 40 is activated. At step 158, the failed line card 40 is deactivated.

5 Proceeding to step 160, the output instruction set 120 corresponding to the failed line card 40, or the first instruction set 120 is associated with the input instruction set 120 corresponding to the activated line card 40 in the redirection memory 114. At step 158, the
10 output instruction set 120 corresponding to the activated card 40, or second instruction set 120, is associated with the input instruction set 120 corresponding to the failed line card 40 in the redirection memory 114. Accordingly, the activated line card 40 will perform the
15 instructions in place of the failed line card 40. The failed line card 40 will perform the instructions of the activated line card 40, which may cross connect low priority traffic supported on an as available basis or may be a null set. In this way, protection switching is
20 provided with minimal processor operations and in minimal time.

 Although the present invention has been described with several embodiments, various changes and modifications may be suggested to one skilled in the art.
25 It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method for providing instructions to a switch, comprising:

- 5 generating a count value including a first portion and a second portion, the second portion operable to identify a relative location in one of a plurality of instruction sets in an instruction memory for a switch;
- determining a redirection value for the first
10 portion of the count value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory; and
- reading an instruction from the relative
15 location in the instruction set based on the redirection value and the second portion of the count value.

2. The method of Claim 1, wherein the first portion of the count value identifies an initial instruction set disparate from the instruction set.

20

3. The method of Claim 1, wherein the count value is a unitary value and the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant
25 bits (LSB) of the unitary value.

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4. The method of Claim 1, further comprising:

incrementing the count value from an initial value to a final value representing a total number of instructions in the instruction memory, each count value including the first portion and the second portion, the second portion identifying a relative location in one of the instruction sets;

for each count value, determining a redirection value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory; and

reading an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

5. The method of Claim 1, wherein the switch is a synchronous switch.

6. The method of Claim 5, wherein the synchronous switch is a time slot interchanger (TSI).

7. A system for providing instructions to a switch, comprising:

a computer-readable medium; and
software stored on the computer-readable
5 medium, the software operable to generate a count value
including a first portion and a second portion, the
second portion operable to identify a relative location
in one of a plurality of instruction sets in an
instruction memory for a switch, to determine a
10 redirection value for the first portion of the count
value based on the first portion of the count value, the
redirection value operable to identify an instruction set
in the instruction memory, and to read an instruction
from the relative location in the instruction set based
15 on the redirection value and the second portion of the
count value.

8. The system of Claim 7, wherein the first portion the count value identifies an initial instruction set disparate from the instruction set.

9. The system of Claim 7, wherein the count value is a unitary value and the first portion comprises a set of most significant bits (MSB) of the unitary value and the second portion comprises a set of least significant bits (LSB) of the unitary value.

10. The system of Claim 7, the software further operable to increment the count value during a cycle of the synchronous switch from an initial value to a final value representing a total number of instructions in the instruction memory, each count value including the first portion and the second portion, the second portion identifying a relative location in one of the instruction sets, to determine for each count value a redirection value based on the first portion of the count value, the redirection value identifying an instruction set in the instruction memory, and to read for each count value an instruction from the relative location in the instruction set based on the redirection value and the second portion of the count value.

11. The system of Claim 7, wherein the switch is a synchronous.

12. The system of Claim 11, wherein the synchronous switch is a time slot interchanger (TSI).

13. A method for associating routing parameters for a switch with line cards serviced by the switch, comprising:

programming a redirection memory to associate a
5 routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of routing parameters to be provided to the switch to service the first line card; and

10 in response to an event initiating activation of a second line card in place of the first line card, reprogramming the redirection memory to associate the routing parameter set in the routing memory with the second line card.

15 14. The method of Claim 13, wherein the event is a failure of the first line card.

15. The method of Claim 13, further comprising:
20 programming the redirection memory to associate a second routing set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card;
25 and

in response to the event initiating activation of the second line card in place of the first line card, reprogramming the redirection memory to associate the second routing parameter set with the first line card.

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16, The method of Claim 13, wherein the routing parameters comprise instructions, the routing parameter set comprises an instruction set and the routing memory comprises an instruction memory.

5

17. The method of Claim 16, wherein the switch comprises a synchronous switch.

18. The method of Claim 17, wherein the synchronous
10 switch is a time slot interchanger (TSI).

19. The method of Claim 13, wherein the redirection
memory comprises a programmable table storing
associations between line cards serviced by the switch
15 and the routing parameter sets in the routing memory for
the switch.

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25. The system of Claim 24, wherein the synchronous switch is a time slot interchanger (TSI).

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28. A system for associating routing parameters for a switch with line cards serviced by the switch, comprising:

means for programming a redirection memory to
5 associate a routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of parameters to be provided to the switch to service the first line card; and

means for reprogramming the redirection memory
10 to associate the routing parameter set in the routing memory with the second line card in response to an event initiating activation of a second line card in place of the first line card.

15 29. The system of Claim 28, wherein the event is a failure of a first line card.

30. The system of Claim 28, further comprising:

means for programming the redirection memory to
20 associate a second routing parameter set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card; and

25 means for reprogramming the redirection memory to associate the second routing parameter set with the first line card in response to the event initiating activation of the second line card in place of the first line card.

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METHOD AND SYSTEM FOR REPROGRAMMING
INSTRUCTIONS FOR A SWITCH

5 ABSTRACT OF THE DISCLOSURE

 The method and system for reprogramming instructions
for a switch includes programming a redirection memory to
associate a routing parameter set in a routing memory for
the switch with a first line card. The routing parameter
10 set includes a plurality of routing parameters to be
provided to the switch to service the first line card.
In response to an event initiating activation of a second
line card in place of the first line card, the
redirection memory is reprogrammed to associate the
15 routing parameters set in the routing memory with the
second line card.

20

25

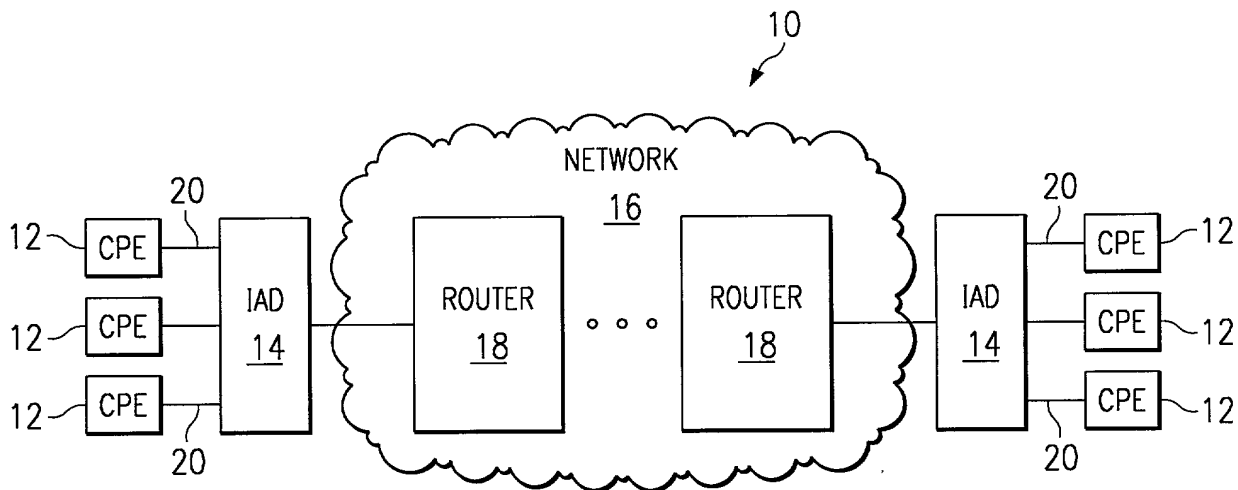


FIG. 1

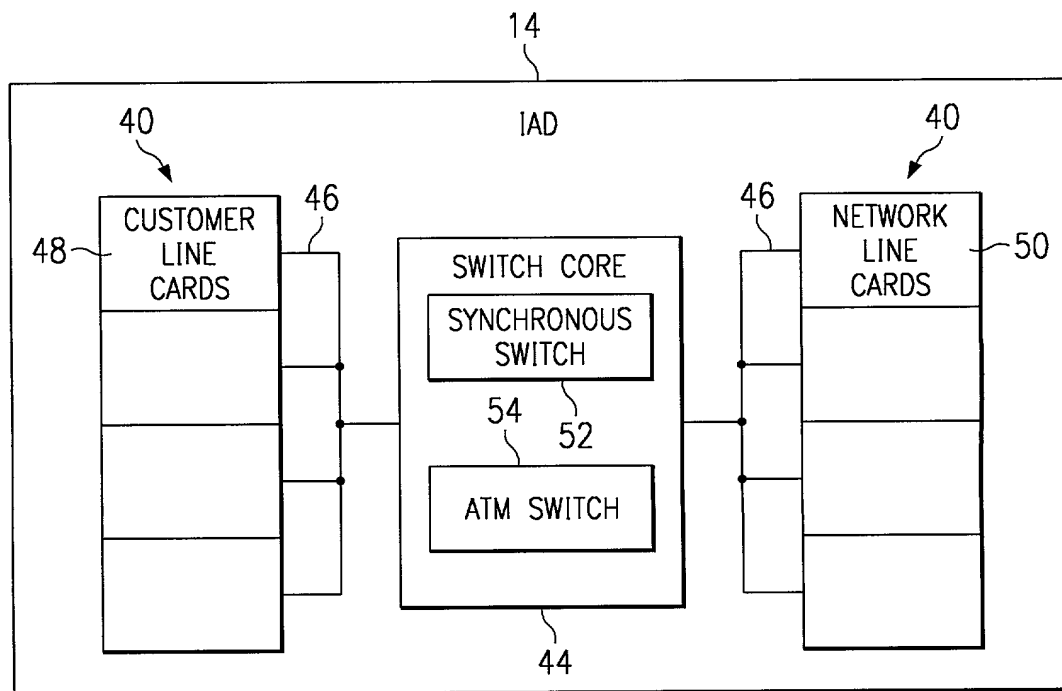


FIG. 2

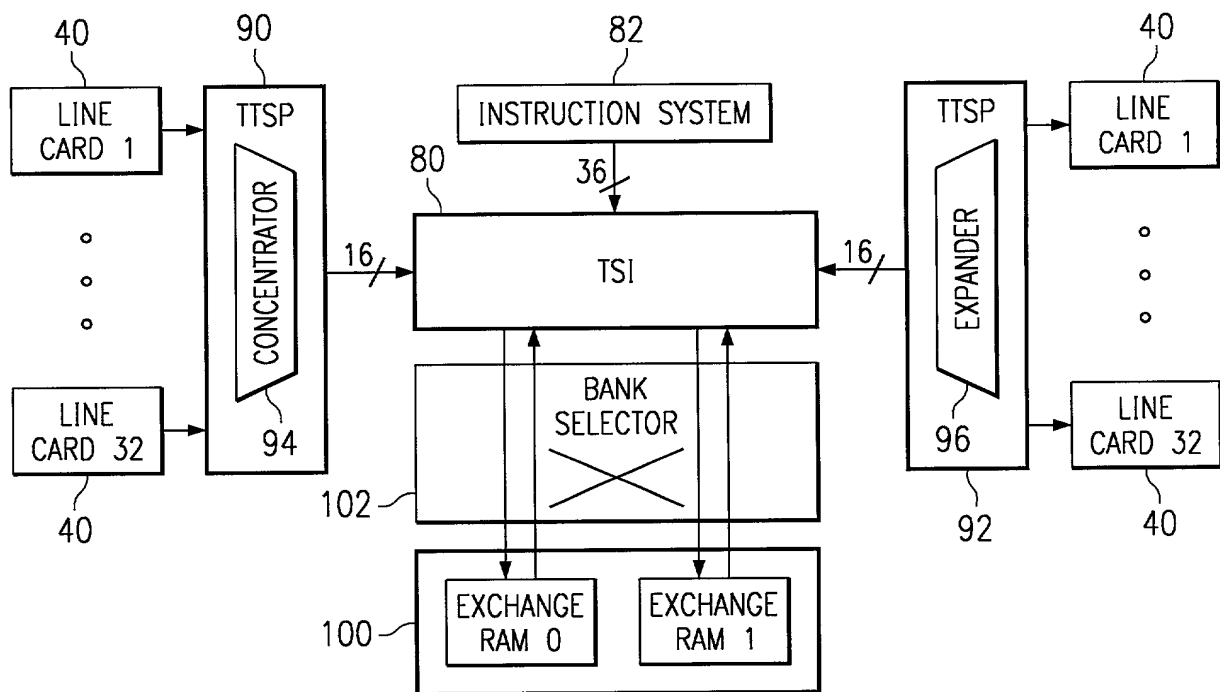


FIG. 3

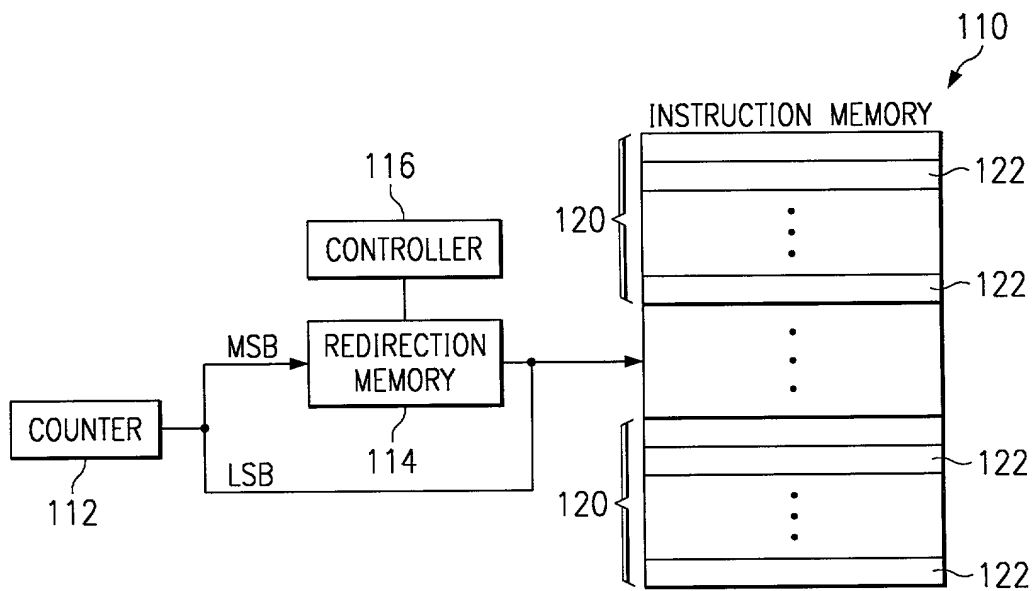


FIG. 4

114 ↗

REDIRECTION MEMORY ↗ 130

INSTRUCTION SET (LINE CARD) 1	INSTRUCTION SET 1
INSTRUCTION SET (LINE CARD) 2	INSTRUCTION SET 30
INSTRUCTION SET (LINE CARD) 3	INSTRUCTION SET 3
⋮	⋮
INSTRUCTION SET (LINE CARD) 30	INSTRUCTION SET 2
INSTRUCTION SET (LINE CARD) 31	INSTRUCTION SET 31
INSTRUCTION SET (LINE CARD) 32	INSTRUCTION SET 32

↗ 132 ↗ 134

FIG. 5

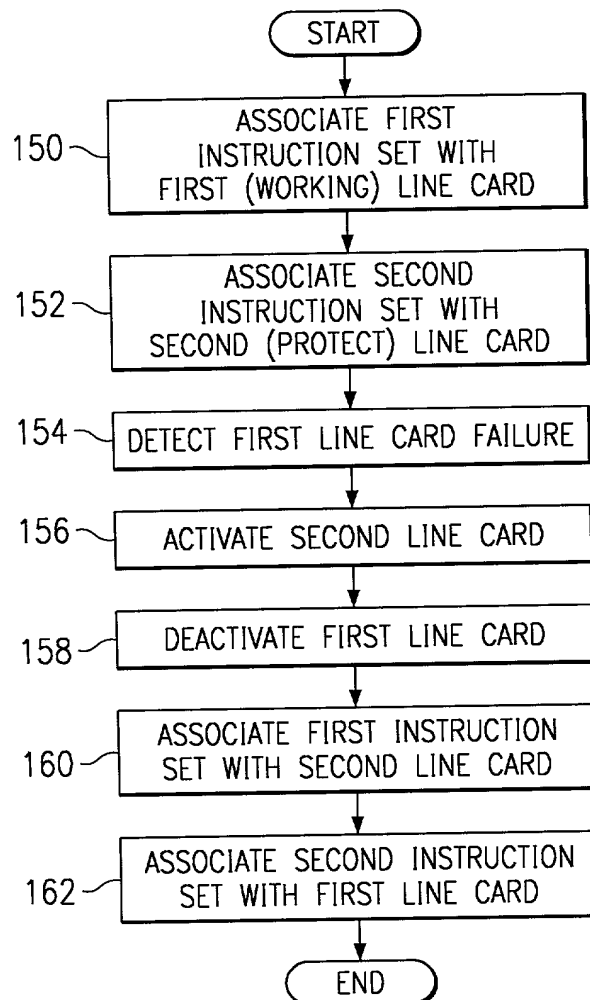


FIG. 6

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; that I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention or design entitled METHOD AND SYSTEM FOR REPROGRAMMING INSTRUCTIONS FOR A SWITCH, the specification of which (check one):

 X is attached hereto; or
 was filed on as Application Serial No. and was
amended on (if applicable);

that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; and that I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Number</u>	<u>Country</u>	<u>Date Filed</u>	<u>Priority Claimed (Yes) (No)</u>
-----NONE-----			

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

<u>Application</u> <u>Serial Number</u>	<u>Date Filed</u>	<u>Status</u>
--	-------------------	---------------

-----NONE-----

I hereby appoint:

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Rodger L. Tate	Reg. No. 27,399
Scott F. Partridge	Reg. No. 28,142
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James Remenick	Reg. No. 36,902
Jay B. Johnson	Reg. No. 38,193
Robert W. Holland	Reg. No. 40,020
Floyd B. Chapman	Reg. No. 40,555
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all of the firm of Baker Botts L.L.P., my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of the sole inventor

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